Modeling Nanoelectronic CNN Cells: CMOS, SETs and QCAs

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Abstract

We investigate the use of nanoelectronic structures in cellular nonlinear network (CNN) architectures, for future high-density and low-power CMOS-nanodevice hybrid circuits. We present simulation results for Single Electron Tunneling (SET) transistors configured as a voltage-to-current transducer for CNN cells. We also present an example of quantum-dot cellular arrays which may be used to realize binary CNN algorithms.

1 Introduction

Nanoelectronics offers the promise of ultra-low power and ultra-high integration density. Several device structures have been proposed and realized experimentally, yet the main challenge remains the organization of these devices in new circuit architectures. For an introduction into this problem area, see the review paper in the previous ECCTD meeting [1].

Here, we investigate the use of nanodevices in cellular nonlinear network (CNN) architectures [2]. Specifically, we focus on nanostructures based on single-electron tunneling (SET) devices [3] and Coulomb-coupled quantum-dot arrays, the so-called Quantum-Dot Cellular Automata (QCA) [4-6].

CNN-type architectures for nanostructures are motivated by the following considerations: On the one hand, locally-interconnected architectures appear to be natural for nanodevices where some of the connectivity may be provided by direct physical device-device interactions. On the other hand, CNN arrays with sizes on the order of 1000-by-1000 (which are desirable for applications such as image processing) will require the use of nanostructures since such integration densities are beyond what can be achieved by scaling conventional CMOS devices.

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2 Single-Electron Tunneling (SET) Transistors

Single-Electron Tunneling (SET) transistors [3] have attractive properties which make them excellent candidates for implementing ultra-dense and complex signal and image processing systems. SET devices satisfy hardware requirements for large-scale neural networks such as local interconnectivity, small device size and low power consumption. Current fabrication technology allows the integration of 10^{11} SET transistors per cm^2 and a power consumption of 10^{-9} W per transistor [7]. Ultimately the goal is to build SET transistors capable of operation at room temperature, and compatible with conventional CMOS process technology. The potential for very dense arrays of SET transistors make them attractive for the realization of CNN circuits, where locally-connected cells may alleviate the necessity for individual external interconnects to every cell.

Figure 1 shows a schematic of a SET transistor, which consists of two tunnel junctions characterized by a junction capacitance, C, and a tunneling resistance, R. The two junctions are separated by a conducting 'island' (or floating contact) which is coupled capacitively to a gate bias, while a source-drain bias is applied across the tunnel junctions as shown.
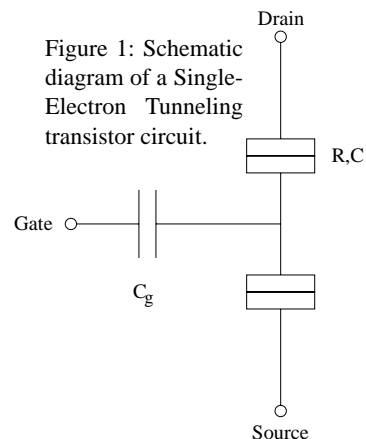
Figure 1: Schematic diagram of a Single-Electron Tunneling transistor circuit.

The I-V characteristics are shown in Fig. 2. The characteristics are calculated using two different techniques, one using SIMON1.1, a single electron circuit simulator based on a Monte Carlo simulation of tunneling
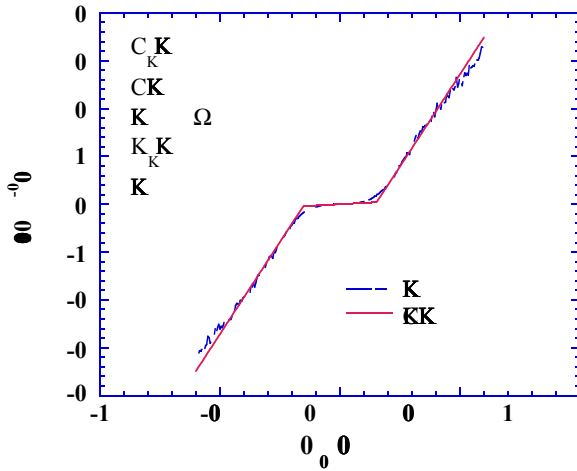
Figure 2a. Drain current of a SET transistor (Fig. 1) as a function of drain-source voltage. The dashed curve represents the simulated results for the parameters shown obtained from SIMON. The solid curve is the SPICE model fit to the SIMON result.
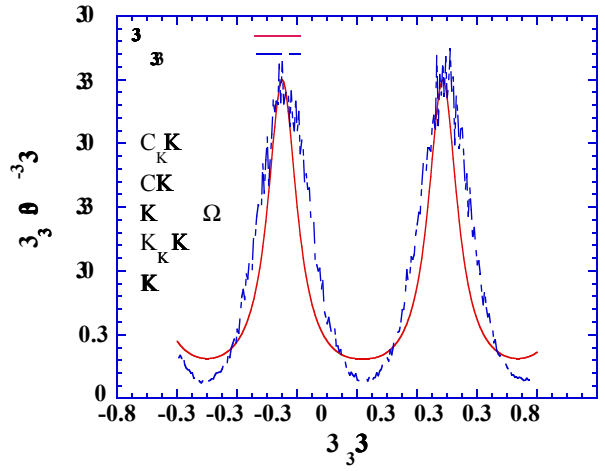

Figure 2b. Drain current versus gate bias for the SET transistor of Fig. 1. The solid curve is the SPICE result while the dashed curve represents the SIMON simulation for this structure.

events through each junction [8]. The second is through SPICE using the SET transistor equivalent circuit proposed by Yu et al. [9]. The advantage of the second model is its compatibility with conventional MOS transistor modeling, and hence the ability to model hybrid MOS/SET transistor circuits. Here the parameters of the SPICE model are chosen to approximate the SIMON characteristics, which represent a more accurate treatment of the physics.

For the SET transistor to operate at room temperature, the tunnel capacitances are chosen to be on the order of 10^{-19} F, such that the single electron charging energy, $e^2/2C > k_b T$. Future reductions of the device dimension are predicted to reach such small capacitances, and hence allow room-temperature operation.

Characteristic of single electron transistors is the so called Coulomb blockade regime around the origin shown in Fig. 2a, where the current is suppressed by the charging energy due to the storage of a single electron in the island surrounded by the two tunnel junctions. This Coulomb blockade region is lifted by an external gate bias capacitively coupled to the island which aligns the Fermi energy in the source and drain contacts with the unoccupied states in the island with energy greater than the Coulomb charging energy, which results in the periodic behavior shown in Fig. 2b as successive electrons are added to the dot.

In CMOS technology, the building block of CNN is a summing node coupled to a transconductance element (voltage-to-current transducer) which switches nonlinearly between two stable operating points, some-
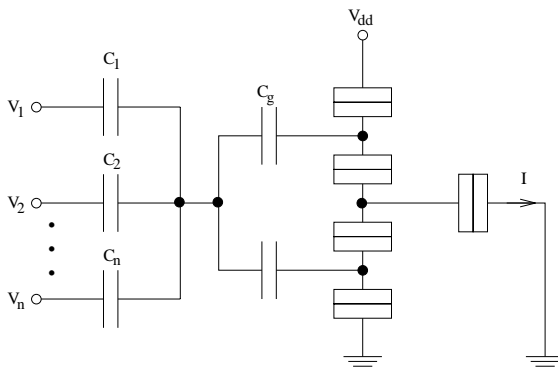

Figure 3a. Schematic structure of a SET summing node/ transducer element for application in CNN circuits.
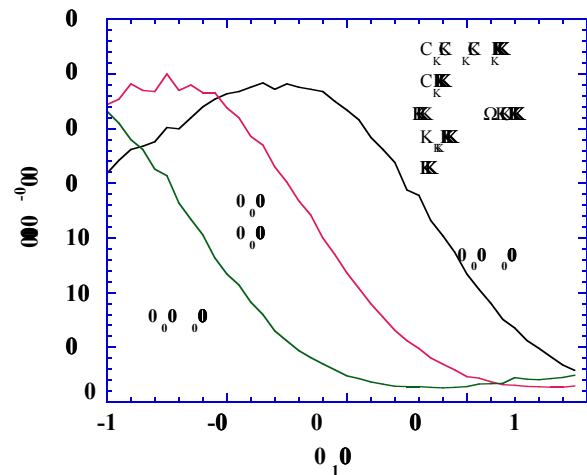

Figure 3b. Simulated results for different input conditions for the circuit in Fig. 3a using SIMON.

what similar to a CMOS inverter [10]. The summing node couples the output and inputs in cells in the adjacent neighborhood to the input of the transducer. A SET realization of this 'neuron' is shown in the schematic of Fig. 3a. A SET inverter [11] forms the basis of a transducer element, with an additional tunnel junction for providing a current proportional to the output voltage. Multiple capacitive inputs to the inverter itself act as a summing node such that the input voltage is the weighted sum of the external voltages, with weights determined by the capacitance values of each input. The output characteristics as a function of various input conditions is shown in Fig. 3b, simulated using SIMON1.1. As can be seen, a bi-stable behavior is obtained dependent on the sum of the input voltages to the transducer node. Our simulations indicate that such a simple threshold circuit may provide the basis for nanoelectronic CNN architectures, which are currently under investigation.

3 Quantum-Dot Cellular Automata (QCA)

Next, we present a QCA implementation of a connected-component detector (CCD), with a simple two-dimensional image-processing algorithm which is tailor-made for the quantum-dot realization. As shown in Fig. 4a, the input is a binary image and the algorithm shifts the image to the right in such a way, that eventually a series of single-dot lines remain; compare Figs. 4b and 4c. In the final image, the number of dots in a given row corresponds to the number of connected parts of the original image in that particular row.

The CCD algorithm can be implemented in a natural way in 2D locally-interconnected cellular structures, such as Cellular Neural Networks (CNN [2]; for the CNN realization of CCD, see [12]) and Quantum-Dot Cellular Automata (QCA [4]). For a quantum-dot-array realization, a fundamental processing element, a *supercell*, must be designed based on QCA cells. A rectangular array of these locally-connected supercells may then be used to implement the CCD function.

Figure 5a shows a schematic diagram of the logic circuit for the supercell, which can be built based on a SET/RESET $S\overline{R}$ flip-flop as a single-bit memory element. Let X_i (i=1,2,...,N) denote the *ith* supercell in a row. (The supercells are connected only to the left and right neighbors, thus we can restrict ourselves to the one-dimensional problem, ignoring row indices.) The logic functions for the inputs to the $S\overline{R}$ flip-flop are as follows; for the SET: $S_i = X_{i-1} \wedge \overline{X_{i+1}} \wedge CLK$, and for the RESET: $\overline{R}_i = X_{i-1} \vee \overline{X_{i+1}} \vee \overline{CLK}$, which can be realized with logic AND, OR and NOT gates. When the CLK signal turns form "0" to "1," then the new state, computed from the previous state of the cell array, is written into the flip-flops. At the boundary, the edge cells are connected to $X_{N+1}=X_0=0$.

The operation of the supercell can be summarized giving the values of X_i in the *(k+1)th* step as the functions of X_i and its two neighbors in the *kth* step:

$$X_i^{k+1} = \begin{cases} X_i^k, \text{ if } \left(X_{i-1}^k X_i^k X_{i+1}^k \right) = 101 \quad or \quad 010 \\ X_{i-1}^k, \text{otherwise} \end{cases}$$

According to this algorithm, the state of the left neighbor is copied to the cell unless the left neighbor, the cell and the right neighbor have the 101 or the 010 state. In these cases, the state of the cell does not change, since copying the state of the left neighbor into the cell would lead to 111 or 000; that is, the disappearance of a white (0) island between two black (1) cells or vice versa. This eventually would lead the an incorrect count of the horizontally-connected components.

The QCA supercell realization of this logic circuit is shown in Fig. 5b. Each supercell is connected to its left and right neighbors and to the CLK clock signal. (A CLK=1 pulse enables writing into the flip-flop.) The AND and OR gates are implemented with majority-
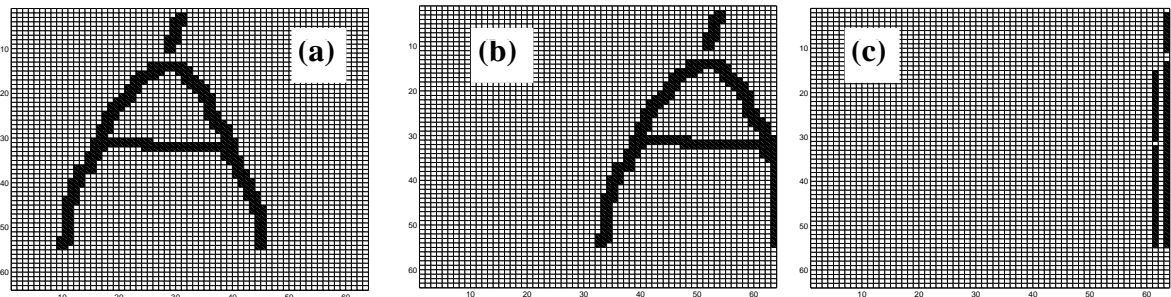

Figure 4. The operation of the Connected Component Detector. (a) The 64x64 input image as the initial state, (b) an intermediate state, and (c) the final state.
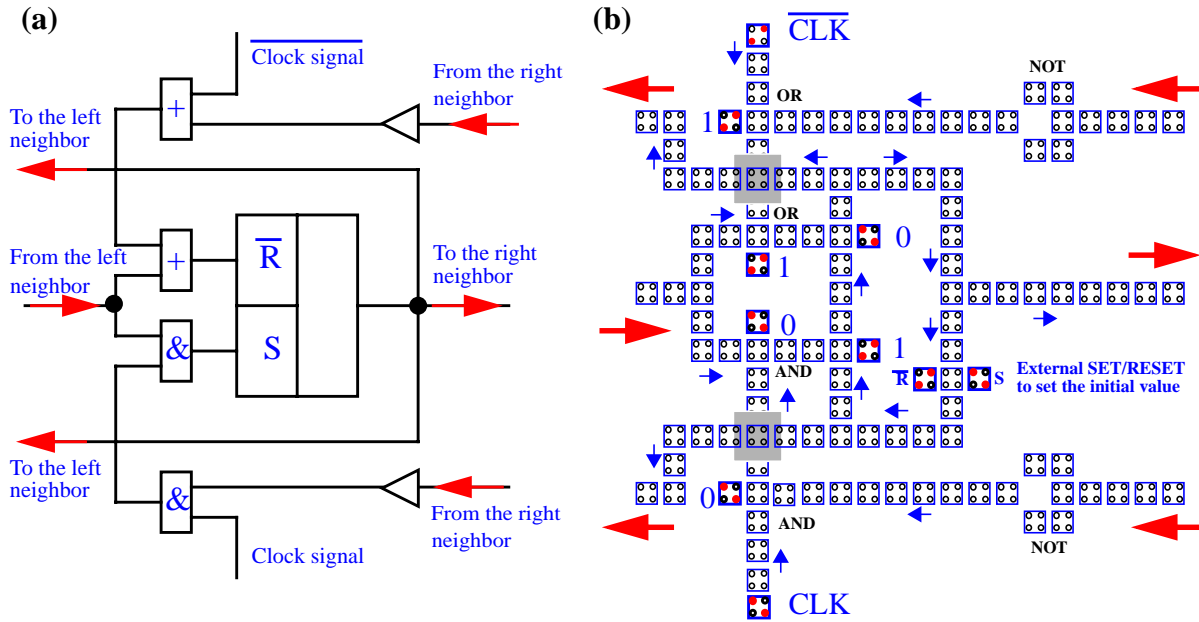
Figure 5. The Connected Component Detector supercell (a) as a logic circuit and (b) realized with an adiabatically clocked QCA circuit.

logic gates. The S$\overline{\text{R}}$ flip-flop is represented by the loop which can be seen in the middle of the circuit. The direction of data propagation is determined by the application of the four-phase adiabatic clocking (not shown here; see [13]) and is indicated by arrows.

Simulations indicate, as illustrated by the example above, that every binary CNN algorithm can be realized by a cellular array composed of adiabatically-clocked QCA supercells.

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